WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising;

a first CMOS logic circuit block capable of being set in one of an active mode and a standby mode; and

a second CMOS logic circuit block capable of being set in one of the active mode and the standby mode;

wherein each of the first and the second CMOS logic circuit blocks includes a first MOS transistor of first conductivity type and a second MOS transistor of second conductivity type serially coupled to the first MOS transistor,

wherein, in the active mode, active current flows through source-drain paths of the first MOS transistor and the second MOS transistor,

wherein, in the standby mode, subthreshold leakage current, which flows through source-drain paths of the first MOS transistor and the second MOS transistor even when a gate-source voltage of one of the first MOS transistor and the second MOS transistor is 0 volts, is reduced, and

wherein both the first circuit block and the second circuit block are set in the standby mode in a first state, and one of the first circuit block and the second circuit block is set in the active mode and another of the first circuit block and the second circuit block is set in the standby node in a second state.

2. The semiconductor integrated circuit device according to claim 1, comprising:

a power supply line for the first CMOS logic circuit and the second CMOS logic circuit;

a third MOS transistor of first conductivity type, a source-drain path of the third MOS transistor being provided between the power supply line and the first CMOS logic circuit; and

a fourth MOS transistor of first conductivity type, a source-drain path of the fourth MOS transistor being provided between the power supply line and the second CMOS logic circuit,

wherein, when the first CMOS logic circuit is set in the active mode, the third MOS transistor is in ON state, when the first CMOS circuit is set in the standby mode, the third MOS transistor is in OFF state, when the second CMOS logic circuit is set in the active mode, the fourth MOS transistor is in ON state, and, when the second CMOS circuit is set in the standby mode, the fourth MOS transistor is in OFF state.

3. The semiconductor integrated circuit device according to claim 2, wherein a source of the third MOS transistor is coupled to the power supply line, a drain of the third MOS transistor is coupled to the source of the first MOS transistor of the first CMOS logic circuit, a source of the fourth MOS transistor is coupled to the power supply line and a drain of the fourth MOS transistor is coupled to the source of the first MOS transistor of the second CMOS logic circuit.

4. The semiconductor integrated circuit device according to claim 3, further comprising:

a fifth MOS transistor serially coupled to MOS transistors of both of the first CMOS logic circuit and the second CMOS logic circuit,

wherein the fifth MOS transistor is in OFF state in the first state and the fifth MOS transistor is in ON state in the second state.

5. The semiconductor integrated circuit device according to claim 4, wherein the fifth MOS transistor has the first conductivity type and a power supply voltage is supplied to the power supply line through a source-drain path through the fifth MOS transistor.

6. The semiconductor integrated circuit device according to claim 5, wherein the drain of the fifth MOS transistor is coupled to the power supply line.

7. The semiconductor integrated circuit device according to claim 2, wherein an absolute value of a threshold voltage of the third MOS transistor is larger than an absolute value of a threshold voltage of the first MOS transistor, and

an absolute value of a threshold voltage of the fourth MOS transistor is larger than the absolute value of the threshold voltage of the first MOS transistor.

8. The semiconductor integrated circuit device according to claim 4, wherein an absolute value of a threshold voltage of the fifth MOS transistor is larger than the absolute value of the threshold voltage of the first MOS transistor.

9. The semiconductor integrated circuit device according to claim 4, wherein a gate width of the fifth MOS transistor is smaller than a total of a gate width of the third MOS transistor and a gate width of the fourth MOS transistor.